REMARKS

Reconsideration and allowance of the subject patent application are respectfully requested.

Claim 25 has been amended to rewrite "units" as "unit" as suggested in the office action and withdrawal of the objection to this claim is respectfully requested.

Claims 26-28 were rejected under 35 U.S.C. Section 112, first paragraph, as allegedly failing to comply with the written description requirement. Applicant respectfully submits that the office action fails to set forth a proper basis for the rejection of these claims.

Claim 26 is rejected because certain recitations therein allegedly "may imply" that "plural second units are disposed in a single physical space between two adjacent first unit circuits." 4/8/2008 Office Action, page 2. Applicant respectfully submits that it is improper to reject a claim on this basis.

The fundamental factual inquiry in determining compliance with the written description requirement is whether the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now claimed. *See, e.g., Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991). See also MPEP 2163.02. While the Examiner contends that claim 26 "may imply" that plural second circuit units are disposed in the physical space between adjacent first circuit units, Applicant submits that

this claim also "may imply" one second circuit unit disposed in the physical space between adjacent first circuit units. The office action contains no allegation that this subject matter is not described in or supported by the written description and, indeed, clearly it is. Consequently, claim 26 is fully and completely described in the subject patent application. The Examiner's suggestion that claim 26 "may imply" or cover other arrangements does not mean claim 26 is not described in the subject patent application. Consequently, withdrawal of the Section 112, first paragraph, rejection of claim 26 is respectfully requested.

Claims 27 and 28 have been amended to recite that the first and second waveform processing circuits recited therein are "each respectively coupled to a single one of" the first and second unit circuits. With respect to the assertions that claim 27 "may imply" plural second waveform processing circuits in the physical space between adjacent first waveform processing circuit and that claim 28 "may imply" plural first and plural second waveform processing circuits in the physical space between first and second circuit units, Applicant reiterates the arguments presented above with respect to claim 26. Specifically, covering these other arrangements does not in and of itself result in a written description issue. Consequently, withdrawal of the rejection of claims 26-28 is respectfully requested.

Because claims 26-28 are not otherwise rejected, these claims are believed to be allowable.

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Claims 1-10 and 12-25 were rejected under 35 U.S.C. Section 102(e) as allegedly being "anticipated" by Azami (U.S. Patent No. 6,702,407).

Applicant respectfully traverses this rejection.

Claim 1 recites a shift register block in which *a first circuit, which is not one of a plurality of spaced-apart, cascade-connected unit circuits of a first shift register, is disposed in the physical space between a unit circuit of a preceding output stage and a unit circuit of a following output stage.*

As previously discussed, Applicant respectfully submits that Figure 3 of Azami (which is referenced in the office action) is a schematic representation and does not reflect the relative physical arrangement of the various components shown therein. In particular, Azami does not disclose (or even suggest) how components of a shift register should be physically arranged or laid out relative to one another and to other circuits. Moreover, even assuming it is erroneously argued that Figure 3 shows a physical arrangement, the inverters and NAND gates are not disposed in the physical space between adjacent flip-flops. Consequently, Azami does not disclose the physical arrangement specified in claim 1 and therefore cannot anticipate claim 1 or any of its dependent claims.

The office action continues to read the schematic diagram of Figure 3 onto the physical arrangement of circuit components recited in the claims. Specifically, the office action contends that "the schematic representation is normally sketched similarly closed

(sic: closely) to the physical arrangement." See 4/8/2008 Office Action, page 11. However, the office action provides no documentary evidence in support of the contention regarding the relationship between schematic and physical arrangements in Azami. In any event, Azami's Figure 3 schematic diagram fails to show that the inverter and logic gate are in the space between adjacent flip-flops. Specifically, the inverter and logic gate are positioned beneath the space between adjacent flip-flops.

The office action further contends that "each of the figures 1 and 10-14 of the pending application is a mere layout example of the driving circuit on a paper ...and does not reflect the actual size and position of each element in the driving circuit." 4/8/2008 Office Action, page 12. Applicant respectfully disagrees. The figures of the subject patent application show the physical arrangement (e.g., position) of circuits (see, e.g., page 16 of the subject patent application describing "layout area in the vertical direction"), while the figures of Azami show how circuit elements are connected to each other. Applicant again respectfully submits that the schematic representation of Azami cannot be used to teach or suggest how the circuit components shown therein are or should be physically arranged.

Claims 8, 9 and 13 also include the above-italicized feature and thus Azami is likewise deficient with respect to these claims and the claims that depend therefrom.

Claim 17 describes unit circuits of a first shift register which are linearly disposed so that physical spaces are provided between each adjacent pair of unit circuits, wherein

circuits other than unit circuits of the first shift register are disposed in the physical spaces between adjacent circuit units. As noted above, Azami does not disclose circuits other than unit circuits disposed in the physical spaces between each adjacent pair of unit circuits as claimed and thus does not anticipate claim 17 or its dependent claims.

Claims 3-5, 18 and 19 recite specific features of the claimed first circuit and the claimed other circuits. The office action merely contends that that the circuit elements in Azami "may be considered" as a processing circuit, a unit circuit for second shift register or a waveform processing circuit. See 4/8/2008 Office Action, page 6. The circuit elements in Azami do not constitute the circuits as alleged in the office action and there is no basis for the rejection of these claims as being made obvious by Azami.

Claims 1-10 and 13-25 were rejected under 35 U.S.C. Section 102(e) as allegedly being "anticipated" by Washio et al. (U.S. Patent No. 6,724,361).

Applicant respectfully traverses this rejection.

The office action points to the Figure 11 embodiment showing inverters 24 between the flip-flops of the shift register. Applicants respectfully submit that Figure 11 of Washio et al. is a circuit diagram (see Washio et al., col. 8, lines 24-25) and does not reflect the relative physical arrangement of the various components shown therein. In particular, Washio et al. does not disclose (or even suggest) how components of a shift register should be physically arranged or laid out relative to one another and to other circuits.

Claims 3-5, 18 and 19 recite specific features of the claimed first circuit and the claimed other circuits. The office action merely contends that that the circuit elements in Washio et al. "may be considered" as a processing circuit, a unit circuit for second shift register or a waveform processing circuit. See 4/8/2008 Office Action, page 8. The circuit elements in Washio et al. do not constitute the circuits as alleged in the office action and there is no basis for the rejection of these claims as being made obvious by Washio et al.

Claim 11 was rejected under 35 U.S.C. Section 103(a) as allegedly being made "obvious" by Azami. Applicants traverse the contentions in the office action that the features of claim 11 would have been obvious in view of Azami. In any event, Azami is deficient with respect to the physical layout specified in claim 9, from which claim 11 depends. Consequently, Applicant submits that claim 11 patentably distinguishes from Azami.

Claims 11 and 12 were rejected under 35 U.S.C. Section 103(a) as allegedly being made "obvious" by Washio et al. Applicant traverses the contentions in the office action that the features of claims 11 and 12 would have been obvious in view of Washio et al. In any event, Washio et al. is deficient with respect to the physical layout specified in claim 9, from which claims 11 and 12 each depends. Consequently, Applicant submits that claims 11 and 12 patentably distinguish from Washio et al.

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The pending claims are believed to be allowable and favorable office action is respectfully requested. Should the Examiner feel that further discussion would facilitate allowance of this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,
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